PROBING SEMICONDUCTOR

PCT5801 Probe Card Test System

A test system, not a probe card analyzer

PCT5801 sits between the ATE and the probe card, forming an end-to-end test path across full-function ATE, relay matrix, motherboard and card. It reproduces the project's specified tester electrical resources, motherboard routing and control-resource conditions rather than performing static resistance measurement alone, which is why it covers open, short, nA-level leakage, control resources and TDR transfer time.

Key figures

67,000	Card-side pins — Current platform capacity; v2 architecture target 300,000	**256 pin/unit × up to 4 units**	ATE resources — Full-function ATE front end
1,024 ch/piece × up to 64 pieces	Relay matrix — Modular channel expansion	**ZIF / POGO**	Card interface — Bridge Beam contact structure

Evidence tiers: delivered, full-load measured, current platform capacity, architecture target - every figure carries one of them.

System structure and the four quantities

1 - Card-side physical pins	Set by the device; current platform capacity 67,000, v2 architecture target 300,000
2 - Matrix addressable nodes	1,024 channels/board x up to 64 boards = 65,536 addressable in turn
3 - Matrix-scanned test paths	16,384 standard, 65,536 maximum configuration
4 - Concurrent instrument resources	Set by the fitted PMU/DPS/digital units, stated in the technical agreement

Specifications

Card-side pins	Current platform capacity 67,000; PCT5801v2 architecture target 300,000	v2 is planned to add PinForce and probe-tip XYZ, correlated with DeepTouch mechanical validation data
ATE resources	256 pin per unit, up to 4 units	Configured for the target card and test items
Relay matrix	1,024 channels per piece, up to 64 pieces	Channel capacity scales with pin count
Motherboard interface	ZIF / POGO with Bridge Beam	Interface form designed per customer card
Control resources	Relay / FPGA / ASIC custom control; MCW (T5830 / T5833); SPI and I^2C (M5 / M7)	Control scheme matched to the tester platform
Analog test	Kelvin four-wire measurement with DPS device power supply	For accurate analog measurement
Configurable resources	Control, source-measure, digital, waveform and capture modules selected per test item	Module specifications are provided in the technical agreement
Virtual instruments	Source and measure, digitizer, scope and spectrum analysis, pin-map visualisation	Software instrument panels
Operator interface	Graphical, customisable GUI	Test flow and display adapt to customer practice
What a channel means	Channel counts are electrical signals on the tester side, not probe-card pins	Keeps channel counts from being read as pin counts
Digital capability	16,384 channels standard; 65,536 maximum configuration (matrix-scanned test paths)	Channels are tester-side scanned signals, not probe-card pins; concurrent instrument resources follow the fitted units
Software tools	Graphical sequence programmer, digital vector editor and debugger, logic analyser, virtual instrument panels, shmoo debugger, automatic VI-curve reports	Supplied with the system
Data and reports	The recipe system supports reuse and archiving, with automatic report generation	Data interfaces are agreed in the technical agreement
Site conditions	Air cooled; 15 to 30 °C, 30 to 70 % RH; AC 220 V 50/60 Hz	Nominal for the base configuration; varies with configuration

Test workflow

Open test	Continuity across all channels with every pin open
Short test	All pins on a short plate to detect channel-to-channel shorts
Leakage test	All pin-to-pin measurement against a 10 nA test threshold
Control test	MCW / FPGA / ASIC / I^2C / SPI control-resource verification

Configuration and acceptance notes

Adapted tester platforms — Solution adapted and delivered: Advantest T5830 (440/480), T5833 (520), V93000 and Teradyne Magnum 5. Solution in build: Advantest T5221, CCTech C16/P16/P16+, Teradyne UltraFlex. Solution planned: XB1152, TM8000, SM0X00, M7, T5825.

AC test — The PBDATA test measures transfer time (TDR) across all signal channels; task times follow pin count and configuration and are agreed in the technical agreement.

Capability position — Covers DC, TDR, logic control and mechanical inspection within one system architecture, orchestrated per the ATE, relay-matrix and instrument configuration; general probe card analyzers usually cover only part of this.

Where it has been shown — Shown as a working machine at Semicon China (Shanghai), Semicon Southeast Asia (Singapore) and SWTest (US) in 2025.

Vendor-neutral — The system is configured around each customer's tester, motherboard, probe card and factory interfaces, tied to no single probe-card maker or ATE platform; quality, cost and lead time are set by contract.

Pins versus scan paths — The mapping from card pins to matrix scan paths is designed per card type; 67,000 is the card-side pin-capacity figure and 65,536 the independent scan-path ceiling - different quantities. The PCT5801v2 architecture extending toward 300,000 pins is presented in technical discussions.

Depth of this page — This page carries capability headlines with their evidence tiers; module specifications, task times and delivered-configuration detail are provided in the technical agreement.

Project delivery

Sample evaluation → Technical agreement → FAT → SAT

Contact

Wenlanxin (Shanghai) Semiconductor Technology Co., Ltd. · Probing Semiconductor
4F, Building A, Building 5, No. 6818 Daye Road, Jinhui Town, Fengxian District, Shanghai
kenny@probing.com.cn · +86 13795427077 · probing.com.cn

Every figure in this sheet carries its basis and evidence tier and is provided for technical evaluation; the configuration, performance and acceptance of a formal project follow the technical agreement both sides confirm. Specifications may change with product iteration.